International
IOR Rectifier

PD - 93930C

IRF6100

HEXFET® Power MOSFET

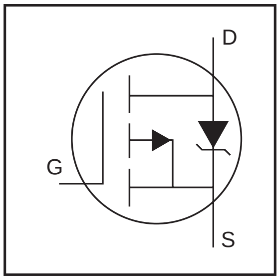
- Ultra Low $R_{DS(on)}$ per Footprint Area
- Low Thermal Resistance
- P-Channel MOSFET
- One-third Footprint of SOT-23
- Super Low Profile (<.8mm)
- Available Tested on Tape & Reel

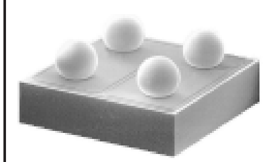
V_{DSS}	$R_{DS(on)}$ max	I_D
-20V	0.065Ω@V_{GS} = -4.5V	-5.1A
	0.095Ω@V_{GS} = -2.5V	-4.1A

Description

True chip-scale packaging is available from International Rectifier. Through the use of advanced processing techniques, and a unique packaging concept, extremely low on-resistance and the highest power densities in the industry have been made available for battery and load management applications. These benefits, combined with the ruggedized device design , that International Rectifier is well known for, provides the designer with an extremely efficient and reliable device.

The FlipFET™ package, is one-third the footprint of a comparable SOT-23 package and has a profile of less than .8mm. Combined with the low thermal resistance of the die level device, this makes the FlipFET™ the best device for application where printed circuit board space is at a premium and in extremely thin application environments such as battery packs, cell phones and PCMCIA cards.




FlipFET™ ISOMETRIC

Absolute Maximum Ratings

	Parameter	Max.	Units
V_{DS}	Drain- Source Voltage	-20	V
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 4.5V	±5.1	A
I_D @ T_C = 70°C	Continuous Drain Current, V_{GS} @ 4.5V	±3.5	
I_{DM}	Pulsed Drain Current ①	±35	
P_D @T_C = 25°C	Power Dissipation③	2.2	W
P_D @T_C = 70°C	Power Dissipation③	1.4	
	Linear Derating Factor	17	mW/°C
V_{GS}	Gate-to-Source Voltage	± 12	V
T_J, T_{STG}	Junction and Storage Temperature Range	-55 to + 150	°C

Thermal Resistance

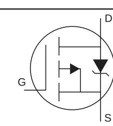
Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JA}$	Junction-to-Ambient③		56.5	°C/W
$R_{\theta J\text{-}PCB}$	Junction-to-PCB mounted	35	——	

9/5/01

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	-20	——	——	V	V_{GS} = 0V, I_D = -250µA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	——	-0.010	——	V/°C	Reference to 25°C, I_D = -1mA
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	——	——	0.065	Ω	V_{GS} = -4.5V, I_D = -5.1A ②
		——	——	0.095		V_{GS} = -2.5V, I_D = -4.1A ②
$V_{GS(th)}$	Gate Threshold Voltage	-0.45	——	-1.2	V	V_{DS} = V_{GS}, I_D = -250µA
g_{fs}	Forward Transconductance	9.8	——	——	S	V_{DS} = -10V, I_D = -5.1A
I_{DSS}	Drain-to-Source Leakage Current	——	——	-1.0	µA	V_{DS} = -20V, V_{GS} = 0V
		——	——	-25		V_{DS} = -16V, V_{GS} = 0V, T_J = 125°C
I_{GSS}	Gate-to-Source Forward Leakage	——	——	100	nA	V_{GS} = 12V
	Gate-to-Source Reverse Leakage	——	——	-100		V_{GS} = -12V
Q_g	Total Gate Charge	——	14	21	nC	I_D = -5.1A
Q_{gs}	Gate-to-Source Charge	——	1.9	2.9		V_{DS} = -16V
Q_{gd}	Gate-to-Drain ("Miller") Charge	——	5.0	7.5		V_{GS} = -5.0V
$t_{d(on)}$	Turn-On Delay Time	——	12	——	ns	V_{DD} = -10V
t_r	Rise Time	——	12	——		I_D = -1.0A
$t_{d(off)}$	Turn-Off Delay Time	——	50	——		R_G = 5.8Ω
t_f	Fall Time	——	50	——		V_{GS} = -4.5V ②
C_{iss}	Input Capacitance	——	1230	——	pF	V_{GS} = 0V
C_{oss}	Output Capacitance	——	250	——		V_{DS} = -15V
C_{rss}	Reverse Transfer Capacitance	——	180	——		ƒ = 1.0MHz, See Fig. 5

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	——	——	-2.2	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ①	——	——	-33		
V_{SD}	Diode Forward Voltage	——	——	-1.2	V	T_J = 25°C, I_S = -2.2A, V_{GS} = 0V ②
t_{rr}	Reverse Recovery Time	——	48	72	ns	T_J = 25°C, I_F = -2.2A
Q_{rr}	Reverse RecoveryCharge	——	34	51	nC	di/dt = 100A/µs ②

Notes:

① Repetitive rating; pulse width limited by max. junction temperature.

② Pulse width ≤ 400µs; duty cycle ≤ 2%.

③ When mounted on 1 inch square 2oz copper on FR-4.

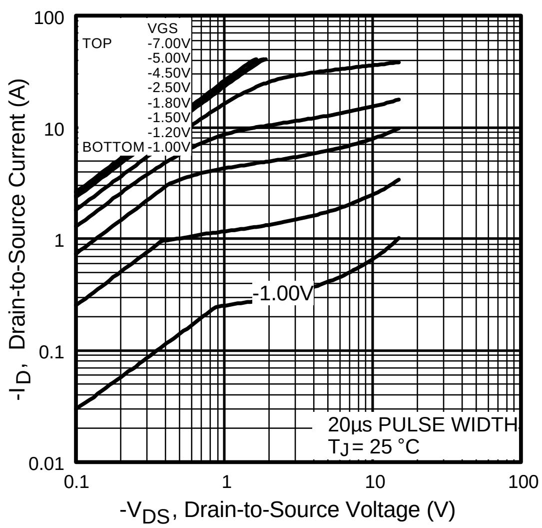


Fig 1. Typical Output Characteristics

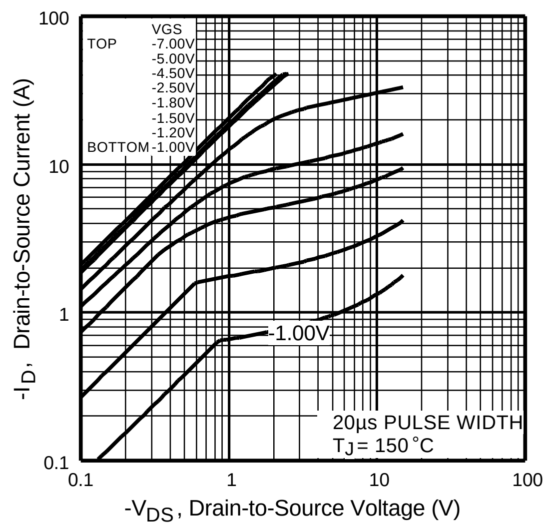


Fig 2. Typical Output Characteristics

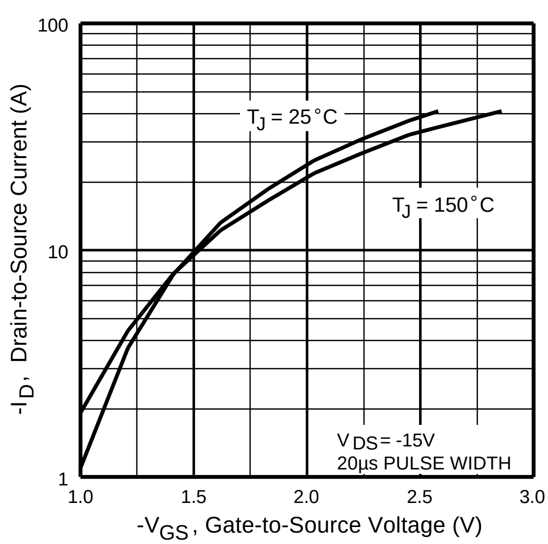


Fig 3. Typical Transfer Characteristics

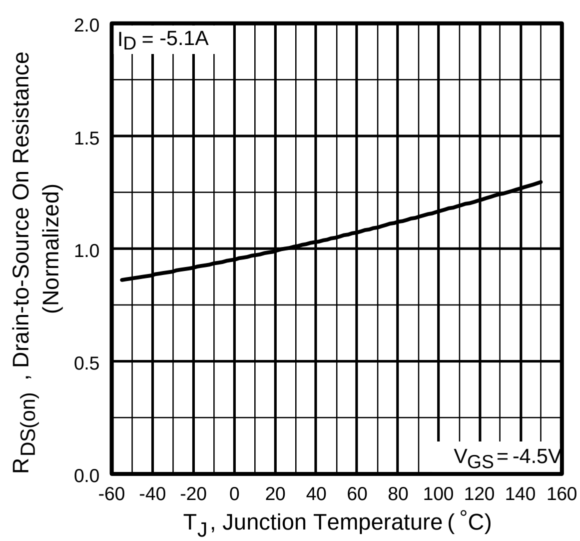


Fig 4. Normalized On-Resistance Vs. Temperature

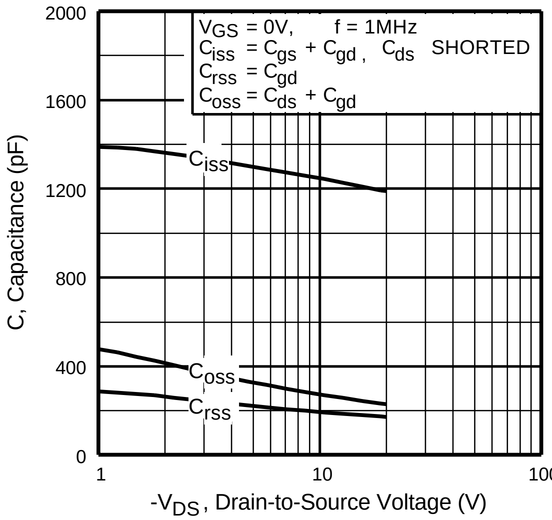


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

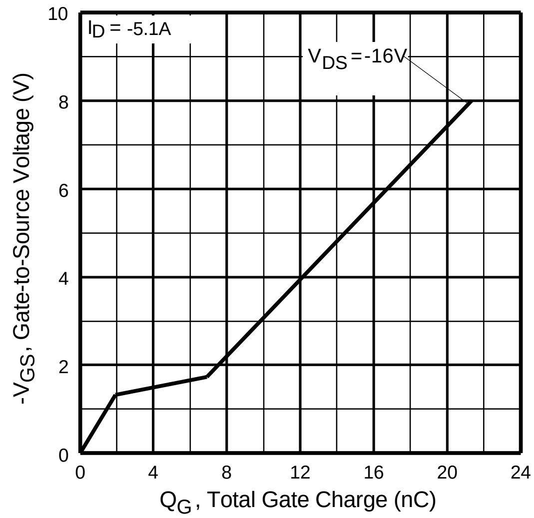


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

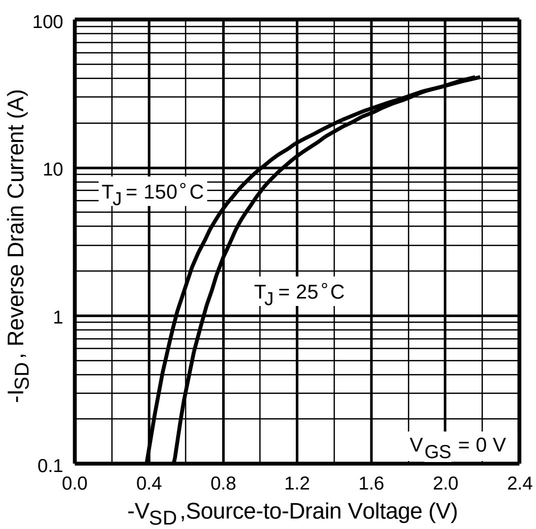


Fig 7. Typical Source-Drain Diode Forward Voltage

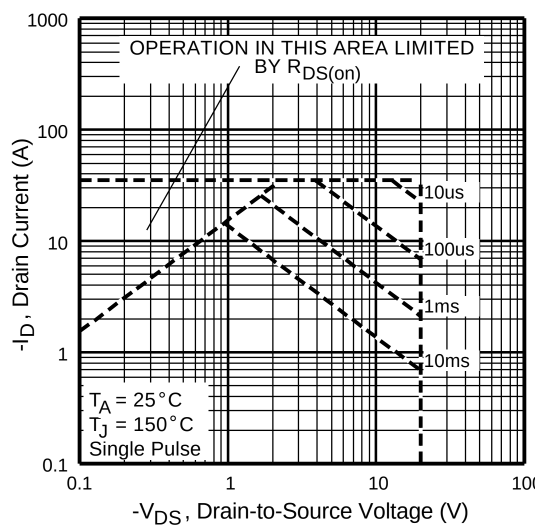


Fig 8. Maximum Safe Operating Area

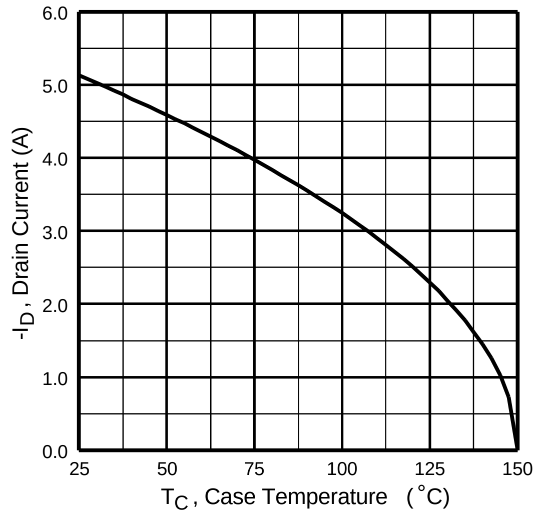


Fig 9. Maximum Drain Current Vs. Case Temperature

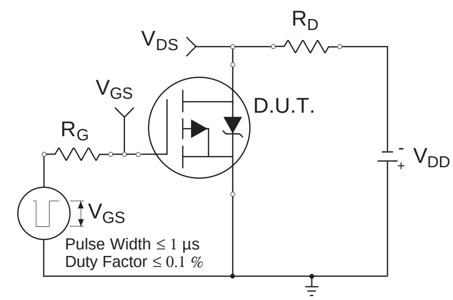


Fig 10a. Switching Time Test Circuit

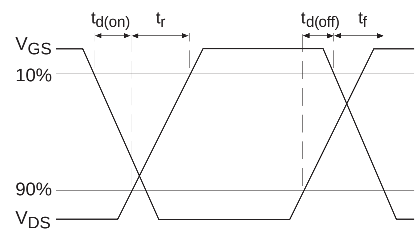


Fig 10b. Switching Time Waveforms

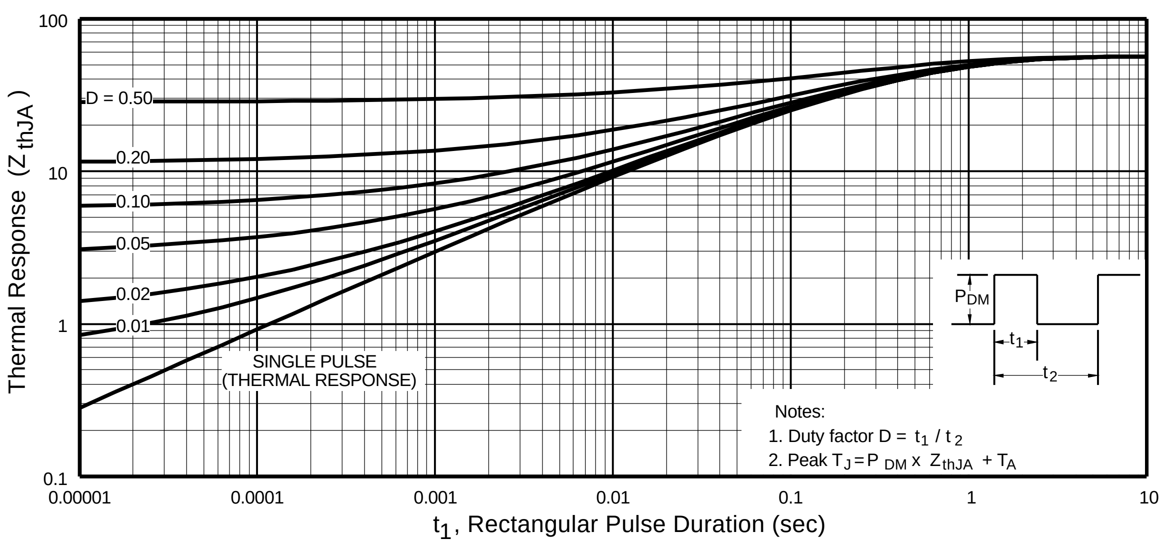


Fig 11. Typical Effective Transient Thermal Impedance, Junction-to-Ambient

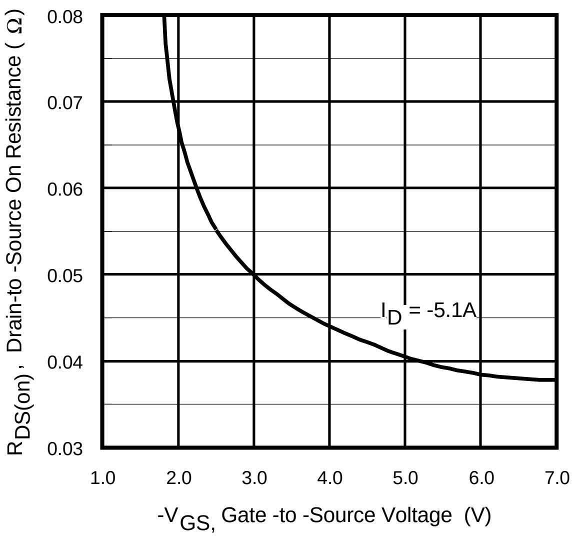


Fig 12. Typical On-Resistance Vs. Gate Voltage

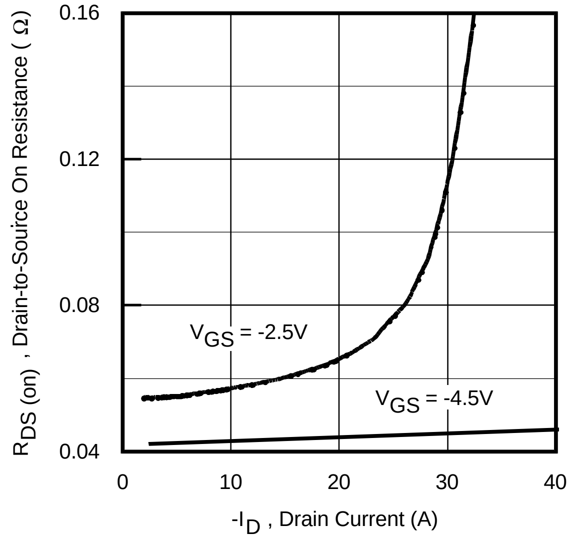


Fig 13. Typical On-Resistance Vs. Drain Current

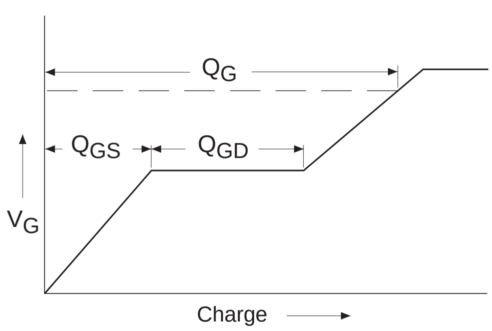


Fig 14a. Basic Gate Charge Waveform

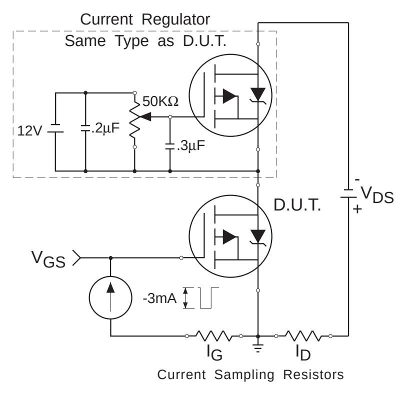


Fig 14b. Gate Charge Test Circuit

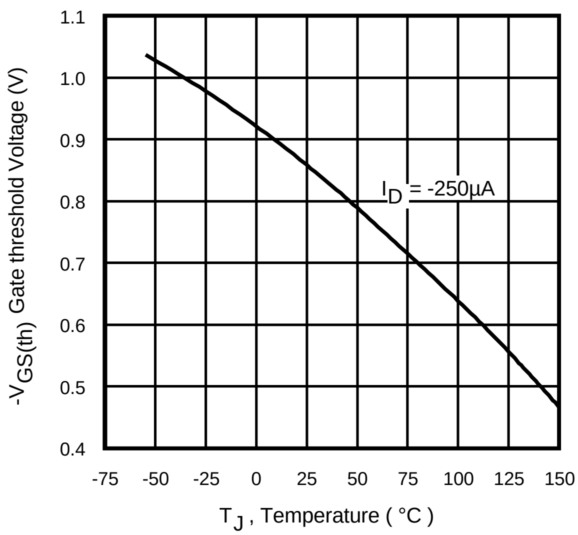


Fig 15. Threshold Voltage Vs. Temperature

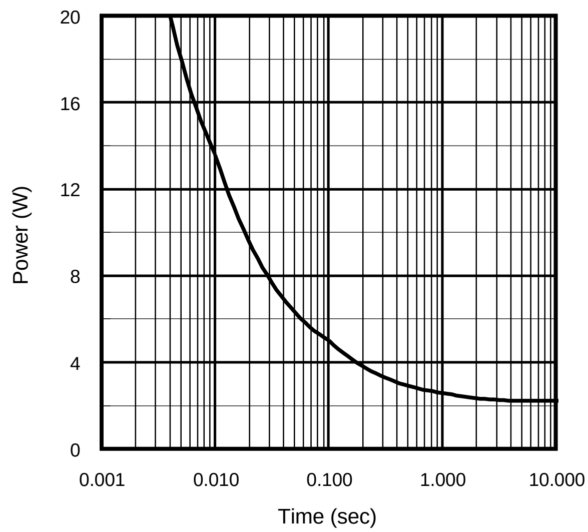
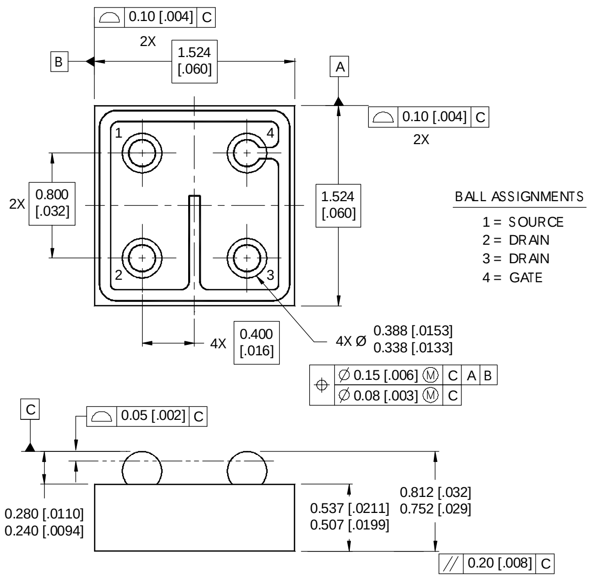
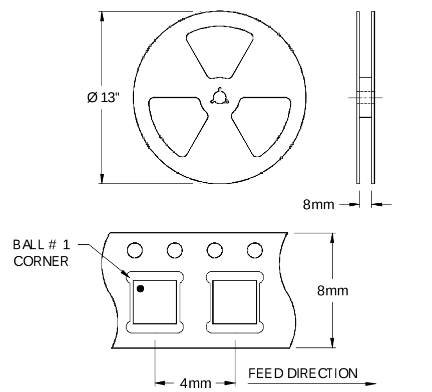


Fig 16. Typical Power Vs. Time

FlipFET™ Outline Dimension and Tape and Reel

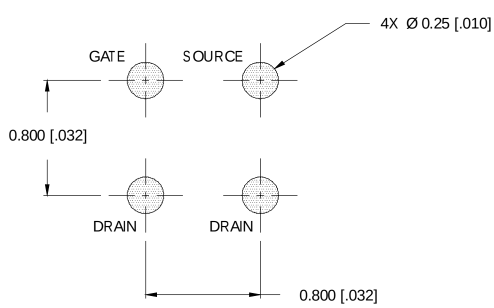




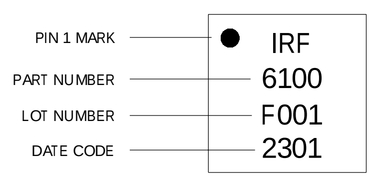
NOTES:
1. TAPE AND REEL OUTLINE CONFORMS TO EIA-481 & EIA-541.

NOTES:
1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994.
2. CONTROLLING DIMENSION: MILLIMETER
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].

RECOMMENDED FOOTPRINT



PART MARKING



Data and specifications subject to change without notice.
This product has been designed and qualified for the consumer market.
Qualification Standards can be found on IR's Web site.

International
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